

AMENDMENTS TO THE CLAIMS

Listing of claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Currently Amended) A multiplexer circuit converting parallel data into serial data synchronized with an internal clock signal, comprising:
a logic circuit processing the internal clock signal and the parallel data; and
a load circuit and a plurality of switching elements connected in series between a first power source line and a second power source line, wherein each of said switching elements consists of a MIS transistor and is controlled in accordance with an output of said logic circuit.
2. (Original) The multiplexer circuit as claimed in claim 1, wherein the serial data is output from a connection node of said load circuit and said plurality of switching elements.
3. (Original) The multiplexer circuit as claimed in claim 1, wherein said logic circuit comprises a plurality of logic cells provided for respective data signal lines of the parallel data.
4. (Original) The multiplexer circuit as claimed in claim 3, wherein each of said logic cells comprises:

an inverter or a buffer amplifying the parallel data and controlling each of said switching elements; and

a first conductivity type control transistor connected between said inverter or said buffer and said second power source line.

5. (Withdrawn) The multiplexer circuit as claimed in claim 4, wherein said load circuit is a plurality of second conductivity type switching transistors, wherein each of said logic cells further comprises:

an inverter or buffer amplifying the parallel data and controlling each of said second conductivity type switching transistors; and

a second conductivity type control transistor connected between said inverter or buffer and said first power source line.

6. (Withdrawn) The multiplexer circuit as claimed in claim 3, wherein each of said logic cells comprises:

a second conductivity type transistor directly receiving the parallel data; and
a first conductivity type control transistor connected between a signal line where the internal clock signal is supplied and controlling each of said switching elements and said second power source line.

7. (Withdrawn) The multiplexer circuit as claimed in claim 1, wherein said multiplexer circuit outputs differential serial data.

8. (Withdrawn) The multiplexer circuit as claimed in claim 7, wherein said logic circuit comprises:

a plurality of negative logic circuit elements provided for respective data signal lines of the parallel data; and a plurality of positive logic circuit elements.

9. (Withdrawn) The multiplexer circuit as claimed in claim 8, wherein each of said negative logic circuit elements comprises:

an odd number of inverters amplifying the parallel data, outputting negative logic data, and controlling said switching elements for the negative logic; and
a first conductivity type control transistor connected between output terminals of said inverters and said second power source line, and

wherein said each of said positive logic circuit elements comprises:

an even number of inverters amplifying the parallel data, outputting positive logic data, and controlling said switching elements for the positive logic; and
a first conductivity type control transistor connected between the output terminals of said inverters and said second power source line.

10. (Withdrawn) The multiplexer circuit as claimed in claim 9, wherein said switching elements for the positive logic and said switching elements for the negative logic are connected to said second power source line through a common current source.

11. (Currently Amended) The multiplexer circuit as claimed in claim 4 [[1]], wherein the internal clock signal is a multi-phase clock signal signals, and said first conductivity type control transistor is controlled by the multi-phase clock signal signals.

12. (Currently Amended) The multiplexer circuit as claimed in claim 11, wherein the multi-phase clock signal is a signals are four-phase clock signal signals having duty ratio of 50%, and said first conductivity type control transistor controlled by the multi-phase clock signal signals is two MIS transistors controlled by two adjacent clock signals of the four-phase clock signal signals.

13. (Currently Amended) The multiplexer circuit as claimed in claim 11, wherein the multi-phase clock signal is a signals are four-phase clock signal signals having duty ratio of 75%, and said first conductivity type control transistor controlled by the multi-phase clock signal signals is one MIS transistor controlled by one phase clock signal of the four-phase clock signal signals.

14. (Currently Amended) The multiplexer circuit as claimed in claim 11, further comprising:

a clock generation circuit generating the multi-phase clock signal signals from an external clock.

15. (Currently Amended) The multiplexer circuit as claimed in claim 4 [[1]], wherein said load circuit is a plurality of second conductivity type switching transistors, wherein each of said logic cells further comprises:

an inverter or buffer amplifying the parallel data and controlling each of said second conductivity type switching transistors; and

a second conductivity type control transistor connected between said inverter or buffer and said first power source line, wherein said first conductivity type control transistor is an n-channel type MIS transistor, and said second conductivity type control transistor is a p-channel type MIS transistor.

16. (Withdrawn) The multiplexer circuit as claimed in claim 1, wherein:

said plurality of switching elements constitute a plurality of first switching elements;

said load circuit constitutes a plurality of second switching elements; and

the serial data is output from a connection node of said plurality of first switching elements connected in series between said first power source line and said second power source line and said plurality of second switching elements.